06-29-00

A

JC820 U.S. PTO 06/28/00

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MIO 0037 VA
First Inventor or Application Identifier	David L. Chapek
Title	METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON
Express Mail Label No.	EL559197880US

JC820 U.S. PTO 09/605293 06/28/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 20] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]
4. Oath or Declaration [Total Pages 1]
   - a. [ ] Newly executed (original or copy)
   - b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [X] Other: Check $846.00 (filing fee); Initial Information Data Sheet

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 072,262

Prior application information: Examiner S. Mulpuri Group / Art Unit: 2812

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* (Insert Customer No. or Attach bar code label here) 23368 or [ ] *Correspondence address below*

Name	PATENT TRADEMARK OFFICE
Address	
City	State / Zip Code
Country	Telephone / Fax

Name (Print/Type)	Timothy W. Hagan	Registration No. (Attorney/Agent)	29,001
Signature	Timothy W. Hagan	Date	June 28, 2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

Initial Information Data Sheet

Inventor Information

Inventor One Given Name::	David L.
Family Name::	Chapek
Postal Address Line One::	35 Sullivan Street
City::	Nashua
State or Province::	NH
Postal or Zip Code::	03060
Citizenship Country::	USA

Correspondence Information

Name Line One::	Killworth, Gottman, Hagan & Schaeff, L.L.P.
Address Line One::	One Dayton Centre, Suite 500
City::	Dayton
State or Province::	OH
Postal or Zip Code::	45402-2023
Telephone::	(937) 223-2050
Fax::	(937) 223-0724
Electronic Mail::	igell@kghs.com

Application Information

Title Line One::	METHOD FOR CONTROLLING THE MORPHOLOGY
Title Line Two::	OF DEPOSITED SILICON ON A SILICON DIOXIDE
Title Line Three::	SUBSTRATE AND SEMICONDUCTOR DEVICES
Title Line Four::	INCORPORATING SUCH DEPOSITED SILICON
Total Drawing Sheets::	4
Formal Drawings?::	Yes
Application Type::	Utility
Docket Number::	MIO 0037 VA

Representative Information

Registration Number One::	26,397
Registration Number Two::	27,262
Registration Number Three::	29,001
Registration Number Four::	39,564
Registration Number Five::	38,769
Registration Number Six::	33,758
Registration Number Seven::	42,695
Registration Number Eight::	44,494
Registration Number Nine::	P-46,867
Registration Number Ten::	P-46,506
Registration Number Eleven::	30,871
Registration Number Twelve::	34,095

Continuity Information

This application is a::	Division of
> Application One::	09/072,262
Filing Date::	May 4, 1998

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant : David L. Chapek

Title : METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON

Docket : MIO 0037 VA

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

EL559197880US

"Express Mail" Mailing Label Number EL559197880US
Date of Deposit June 28, 2000
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231.

Kerrie E. Cela

Kerrie E. Cela
Legal Secretary

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant : David L. Chapek
Title : METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON
Docket No. : MIO 0037 VA

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Please preliminarily amend the above-identified application as follows.

IN THE TITLE

Please delete the title and insert the following new title: --SEMICONDUCTOR DEVICES INCLUDING A LAYER OF POLYCRYSTALLINE SILICON HAVING A SMOOTH MORPHOLOGY--.

IN THE SPECIFICATION

At page 1 after the Title, please insert the following:

--CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. Patent Application Serial No. 09/072,262, filed May 4, 1998.--

IN THE CLAIMS

Please cancel claims 1-8, and 13.

Please amend claims 9-12 and 14 to read as follows:

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process [to provide a layer of polycrystalline silicon, which is subsequently deposited on said layer of silicon dioxide with a smooth morphology]; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide, said layer of polycrystalline silicon having a smooth morphology; and

a source, a drain and a gate formed in said semiconductor substrate to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; and

a gate, a source and a drain for each of said field effect transistors formed on said semiconductor substrate.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted, said layer of polycrystalline silicon having a smooth morphology; and

a repeating series of gates, sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of gates, sources and drains being formed on said semiconductor substrate.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation;

a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate, said layer of polycrystalline silicon having a smooth morphology;

a layer of a insulating material formed on at least a portion of said layer of polycrystalline silicon;

a source region and a drain region formed on said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

REMARKS

Claims 9-12 and 14 were withdrawn from the parent application. Applicant respectfully requests examination of those claims on the merits in this divisional application.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, L.L.P.

By _____
Timothy W. Hagan
Registration No. 29,001

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724

TWH/kec

ATTORNEY DOCKET: MIO 037 PA

METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON

The present invention relates to a method for pretreating a silicon dioxide film to provide a polycrystalline silicon film, which is subsequently deposited on the silicon dioxide film, with a smooth morphology.

BACKGROUND OF THE INVENTION

Advancements in semiconductor manufacture have led to increases in the density and miniaturization of microelectronic circuits. As an example, the manufacture of 64 Mb DRAMs is now possible and 256 Mb prototypes are currently being developed. A key requirement for achieving such high device packing density is the formation of increasingly smaller components. One way to make such smaller components is to employ thinner and smoother films when fabricating those components.

Currently in the art, silicon dioxide films are pretreated with hydrogen ions to prepare the surface of the silicon dioxide film for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. The silicon dioxide is pretreated by ion beam bombardment by a Kaufman ion source. Hydrogen ion beam pretreatment is typically performed using a Kaufman ion beam source directed normally to the substrate. A Kaufman ion source employs a metal grid to accelerate ions at a particular target. During an ion implantation process using a Kaufman ion source, metal from the metal grid sputters off of the grid and becomes implanted in the target object causing the target object to become contaminated. As the size of devices on the target object decreases, the effect of damage caused by sputtered metal from the metal grid increases.

Plasma source ion implantation (PSII) has been used to dope various materials, such as tools, aluminum cans and artificial joints, to improve their wear,

friction and corrosion properties. PSII is a process by which ions are implanted into a target at energies high enough to bury the ions below the target's surface. To implant the ions in the target, an ionized plasma is formed about the target in an enclosed chamber. A high voltage pulse is applied to the target relative to the conductive walls of the chamber. Ions from the plasma are then driven into the surfaces of the target from all sides simultaneously without any manipulation of the target.

United States Patent No. 4,764,394 to Conrad teaches one method and apparatus for PSII. Conrad describes that plasma source ion implantations may be performed on complex three-dimensional objects formed from materials such as pure metals, alloys, semi-conductors, ceramics and organic polymers. Conrad describes the process as providing significant increases in surface hardness of metals and ceramics and providing changes in the optical properties and electrical conductivity of organic polymers.

United States Patent No. 5,354,381 to Sheng teaches a plasma immersion ion implantation apparatus which generally is a variation of the apparatus taught by Conrad. The Sheng apparatus uses a pair of power supplies and very short ionization negative pulses applied to the cathode underlying the target in conjunction with or followed by short ionization pulses applied to a second cathode which is facing toward the primary (target) electrode to provide neutralizing electrons.

Thus, a need has developed in the art for a process by which silicon dioxide films can be pretreated to ensure that a subsequently deposited polycrystalline silicon film will be provided with a smooth morphology but without the contamination problems of present processes.

SUMMARY OF THE INVENTION

The present invention solves that current need by providing a method by which a silicon dioxide film is prepared so that a subsequently deposited

polycrystalline film is deposited smoothly and uniformly onto the silicon dioxide film.

One aspect of the present invention is directed to a method for controlling the morphology of deposited silicon on a layer of silicon dioxide. The method comprises the steps of: providing a layer of silicon dioxide; implanting hydrogen ions into the layer of silicon dioxide by plasma source ion implantation; and forming a layer of polycrystalline silicon on the layer of silicon dioxide.

Another aspect of the present invention is directed to a method for pretreating silicon dioxide comprising the steps of: providing a layer of silicon dioxide; and implanting hydrogen ions into a surface of the layer of silicon dioxide by plasma source ion implantation.

Yet another aspect of the present invention is directed to a method for forming a semiconductor device precursor comprising the steps of: providing a semiconductor substrate; forming a layer of silicon dioxide on the semiconductor substrate; implanting hydrogen ions by plasma source ion implantation into the layer of silicon dioxide; and forming a layer of polycrystalline silicon on the layer of silicon dioxide.

Still another aspect of the present invention is directed to a method for forming a semiconductor device precursor comprising the steps of: providing a semiconductor substrate; forming a layer of silicon dioxide on said semiconductor substrate; exposing said semiconductor substrate to a hydrogen plasma containing hydrogen ions; and applying a high voltage pulse to said semiconductor substrate thereby implanting hydrogen ions from said ionized hydrogen plasma into a surface of said layer of silicon dioxide so that a subsequently formed layer of polycrystalline silicon has a smooth morphology.

An additional aspect of the present invention is directed to a method for forming a semiconductor device precursor comprising the steps of: providing a semiconductor substrate; forming a layer of silicon dioxide on said semiconductor substrate; exposing said semiconductor substrate to a hydrogen plasma containing hydrogen ions; applying a high voltage pulse to said semiconductor substrate to

implant hydrogen ions from said ionized hydrogen plasma into a surface of said layer of silicon dioxide so that a subsequently formed layer of polycrystalline silicon has a smooth morphology; and forming a layer of polycrystalline silicon on said surface of said layer of silicon dioxide.

A further aspect of the present invention is directed to a method for forming a semiconductor device comprising the steps of: providing a semiconductor substrate; forming a layer of silicon dioxide on the semiconductor substrate; implanting hydrogen ions by plasma source ion implantation into the layer of silicon dioxide; and forming a layer of polycrystalline silicon on the layer of silicon dioxide.

Another aspect of the present invention is directed to a method for forming a field effect transistor comprising the steps of: providing a semiconductor substrate having a layer of silicon dioxide formed thereon; implanting hydrogen ions by plasma source ion implantation into the layer of silicon dioxide; forming a layer of polycrystalline silicon on the layer of silicon dioxide; and forming a source, a drain and a gate in the semiconductor substrate to form a field effect transistor.

Still another aspect of the present invention is directed to a method for forming a memory array. The memory array includes a plurality of memory cells arranged in rows and columns with each of the plurality of memory cells including at least one field effect transistor. This method comprises the steps of: providing a semiconductor substrate; forming a layer of silicon dioxide on at least a portion of the semiconductor substrate; implanting hydrogen ions into at least a portion of the layer of silicon dioxide by plasma source ion implantation; forming a layer of polycrystalline silicon over at least the portion of the layer of silicon dioxide into which the hydrogen ions were implanted; and forming a gate, a source and a drain for each of the field effect transistors, on the semiconductor substrate.

Yet another aspect of the present invention is directed to a semiconductor device precursor. The semiconductor device precursor includes a semiconductor substrate. A layer of silicon dioxide is formed on the semiconductor substrate. The layer of silicon dioxide has been doped with hydrogen ions deposited

by a plasma source ion implantation process to provide a subsequently deposited layer of polycrystalline silicon with a smooth morphology. Finally, a layer of polycrystalline silicon is formed on the layer of silicon dioxide.

An additional aspect of the present invention is directed to a field effect transistor. The field effect transistor includes a semiconductor substrate. A layer of silicon dioxide is formed on at least a portion of the semiconductor substrate. The layer of silicon dioxide has hydrogen ions implanted therein by plasma source ion implantation. A layer of polycrystalline silicon is formed on at least a portion of the layer of silicon dioxide. A source, a drain and a gate are also formed in the semiconductor substrate to complete the field effect transistor.

Still yet another aspect of the present invention is directed to a memory array. The memory array comprises a semiconductor substrate. A layer of silicon dioxide is formed on at least a portion of the semiconductor substrate. The layer of silicon dioxide has hydrogen ions implanted into at least a portion of the layer of silicon dioxide by plasma source ion implantation. A layer of polycrystalline silicon is formed over at least the portion of the layer of silicon dioxide into which the hydrogen ions were implanted. A plurality of memory cells are arranged in rows and columns on the semiconductor substrate. Each of the plurality of memory cells comprises at least one field effect transistor. Gates, sources and drains for each of the field effect transistors are also formed on the semiconductor substrate.

A still further aspect of the present invention is directed to a semiconductor wafer. The wafer comprises a wafer including a semiconductor substrate. The wafer is divided into a plurality of die. A layer of silicon dioxide is formed on at least a portion of the semiconductor substrate. On each of the plurality of die the layer of silicon dioxide has hydrogen ions implanted into at least a portion of the layer of silicon dioxide by plasma source ion implantation. A layer of polycrystalline silicon is formed over at least the portion of the layer of silicon dioxide into which the hydrogen ions are implanted. The wafer also includes a repeating series of gates, sources and drains for at least one field effect transistor formed on

each of the plurality of die. The series of gates, sources and drains are formed on the semiconductor substrate.

Another aspect of the present invention is directed to a method for making a thin film transistor. The method comprises the steps of: providing a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass; forming a layer of a gate oxide material on the semiconductor substrate; implanting, by plasma source ion implantation, hydrogen ions into a surface of the semiconductor substrate; forming a layer of polycrystalline silicon on the surface of the semiconductor substrate; forming a layer of an insulating material on the layer of polycrystalline silicon; and forming a source region, a drain region and a gate electrode.

Still another aspect of the present invention is directed to a thin film transistor. The thin film transistor includes a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass. The semiconductor substrate has hydrogen ions implanted therein by plasma source ion implantation. A layer of polycrystalline silicon is formed on at least a portion of semiconductor substrate. A layer of a insulating material is formed on at least a portion of the layer of polycrystalline silicon. A source region and a drain region are formed on the layer of polycrystalline silicon. Finally, a gate electrode is formed on the layer of insulating material.

It is an object of the present invention to provide a method by which a layer of silicon dioxide, which serves as either a semiconductor substrate or another layer on the substrate, can be pretreated so that a subsequently deposited film of polycrystalline silicon can be deposited on the layer of silicon dioxide free of contaminants and have a smooth morphology. It is also object of the present invention to provide various semiconductor parts and devices which include a layer of polycrystalline silicon having a smooth morphology.

Other objects and advantages of the invention will be apparent from the following detailed description, the accompanying drawings and the appended

claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 presents a cross sectional view of semiconductor device precursor formed by the method of the present invention;

Fig. 2 presents a cross sectional view of a field effect transistor formed by the method of the present invention;

Figs. 2A-2C present cross sectional views of various stages in the manufacture of the field effect transistor shown in Fig. 2;

Fig. 3 shows a schematic view of a memory array formed by the method of the present invention;

Fig. 3A shows a schematic view of a memory cell of the memory array shown in Fig. 3;

Fig. 4 shows a schematic view of a wafer manufactured by the method of the present invention; and

Fig. 5 presents a cross sectional view of a thin film transistor formed by the method of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device precursor 10 formed by the method of the present invention is shown in Fig. 1. The precursor 10 includes a semiconductor substrate 12, a layer 14 of silicon dioxide 16 and a layer 18 of polycrystalline silicon 20. The substrate 12 can be formed of any material currently in use in the art to form substrates for semiconductors and integrated circuits. For example, the substrate 12 can be formed from silicon which can be oxidized to form the layer 14 of silicon dioxide 16. Other useful materials for substrate 12 include, but are not limited to, gallium arsenide, indium phosphide, polycrystalline silicon, silicon dioxide, glass and quartz. Glass, quartz and silicon dioxide are particularly useful if the precursor 10 is further processed into a thin film transistor, such as that described

below in connection with Fig. 5.

With continued reference to Fig. 1, the layer 14 of silicon dioxide 16 is formed on the substrate 12 by any conventional oxidation process or deposition process, and has been doped with hydrogen ions to provide a surface conducive to the deposition of polycrystalline silicon. Depending upon the nature of the layer 14 of silicon dioxide 16, the layer 14 of silicon dioxide 16 can be formed by thermal oxidation, chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), metalorganic chemical vapor deposition (MOCVD), and sputtering. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 of silicon dioxide 16 by any deposition process currently used in the art to form a layer of polycrystalline silicon on a layer of silicon dioxide. Useful deposition methods include, but are not limited to, thermal oxidation, CVD, LPCVD, PECVD, MOCVD and sputtering.

The layer 14 of silicon dioxide 16 is doped by plasma source ion implantation (PSII). Plasma source ion implantation is also referred to as plasma doping (PLAD), plasma immersion ion implantation (PI^3) and plasma implantation (PI). As used herein, the term "plasma source ion implantation" incorporates and encompasses "plasma doping," "plasma implantation," and "plasma immersion ion implantation." A useful plasma source ion implantation technique and device are taught in United States Patent No. 4,764,394 to Conrad, which is incorporated herein by reference in its entirety. Using the Conrad technique, the substrate 12 is placed in a chamber which has walls formed from an electrically conductive material. The substrate 12 is placed on an arm which is electrically connected to a high voltage pulse power supply, such as a pulse line-pulse transformer type or a high voltage tube modulated pulser. The chamber is filled with hydrogen gas under a very low pressure in the range of form about 10^{-1} to about 10^{-4} Torr. The gas is then ionized to form a plasma containing hydrogen ions. The plasma can be generated by any of a variety of plasma sources, including, but not limited to, hot filament, radio frequency, electron cyclotron resonance, magneton and glow discharge resulting

from the target bias itself. A large negative pulse with respect to the chamber is applied to the substrate 12 to accelerate ions from the plasma toward the layer 14 of silicon dioxide 16, to create a plasma sheath around the substrate 12, and to implant the ions into the layer 14 of silicon dioxide 16. A plasma density, useful for implanting an appropriate amount of hydrogen ions into the layer 14, ranges from about 10^6 ions/cm^3 to about 10^{11} ions/cm^3.

Another useful plasma source ion implantation apparatus and technique is described in United States Patent No. 5,354,381 to Sheng which is also incorporated herein by reference in its entirety. The Sheng patent describes a technique in which a "cold" cathode is used to generate the hydrogen plasma. In this process, the substrate 12 is mounted on a electrode, which is positioned in a wall of an implantation chamber. A pulsed negative voltage is applied to the electrode which creates electric field lines with the walls of the chamber. These electric field lines cause a hydrogen gas, which has been introduced into the chamber, to ionize and causes positive ions from the hydrogen gas to be accelerated toward the substrate 12 and to become implanted into the substrate 12.

After the hydrogen ions have been implanted into the layer 14 of silicon dioxide 16, the layer 18 of polycrystalline silicon 20 is formed on the layer 14. The layer 18 of polycrystalline silicon 20 is formed on the layer 14 by any deposition method currently in use in the art. Useful deposition methods include, but are not limited to, thermal oxidation, CVD, LPCVD, PECVD, MOCVD and sputtering.

By implanting hydrogen ions into the layer 14 of silicon dioxide 16 by plasma source ion implantation, the resulting layer 18 of polycrystalline silicon 20 is provided with a smooth morphology. By "smooth", it is meant that, when the layer 18 is measured by atomic force microscopy, the layer 18 of polycrystalline silicon 20 has a root mean square (rms) deviation of from about 5 nm to about 12 nm. The method of the present invention provides a layer 18 of polycrystalline silicon 20 which is smoother than either a layer of polycrystalline silicon deposited on a non-treated layer of silicon dioxide (rms=22 nm) or a layer of polycrystalline silicon

deposited on a layer of silicon dioxide pretreated with an H_2 gas bake (rms=33 nm). While not wishing to be bound by a particular theory, it is believed that the implantation of the hydrogen ions in the silicon dioxide substrate increases the number of nucleation sites for polycrystalline silicon deposition thus affecting the morphology of the subsequently deposited layer of polycrystalline silicon.

Unlike a Kaufman ion source implantation technique, a plasma source ion implantation apparatus does not employ a metal grid to accelerate the hydrogen ions toward the target object but instead uses the target object itself, in this case the substrate 12, to accelerate the ions toward the target object. Thus, plasma source ion implantation reduces the possibility of contamination of the target object by eliminating a device which employs a metal grid. Further, plasma source ion implantation can be used on smaller devices or substrates than a Kaufman ion source without increasing the likelihood for contamination of the target object.

The semiconductor device precursor 10 of the present invention can be used to form any semiconductor device which requires that a layer of polycrystalline silicon be formed over a layer of silicon dioxide. Exemplary semiconductor devices which can be formed from the semiconductor precursor 10 include, but are not limited to, field effect transistors, thin film transistors, dynamic random access memory devices (DRAMs), static random access memory devices (SRAMs), memory arrays and semiconductor wafers.

Fig. 2 presents a cross sectional view of a field effect transistor 50 formed by the method of the present invention. The field effect transistor 50 is formed on a semiconductor substrate 52, which is desirably silicon dioxide, quartz or glass. The field effect transistor 50 includes a gate oxide 54, a source 56 and a drain 58. The gate oxide 54, the source 56 and the drain 58 are formed in the substrate 52. A layer 64 of polysilicon 66 is formed on the gate oxide 54 to form a gate electrode 70. A pair of spacers 68 are formed on the sides of the layer 64 of polysilicon 66. A layer 72 of a field oxide 74 is also formed on the substrate 52.

The substrate 52 can be formed of any material currently in use in the

art to form substrates for semiconductors and integrated circuits. Desirably, the substrate 52 is formed from silicon which can be oxidized to form the layer 72 of field oxide material 74. Other useful substrates 52 include, but are not limited to, gallium arsenide, indium phosphide, polycrystalline silicon, germanium, silicon dioxide, glass and quartz. As used herein, the term "substrate" is not limited to bulk substrate materials but can also denote thinner substrates such as those used to form thin film transistors. One skilled in the art will appreciate that substrate 52 can be layer or part of a larger semiconductor device.

A method for making the field effect transistor 50 is shown in Figs. 2A-2C. As an initial step, the layer 72 of the field oxide 74 is formed on the substrate 52 by means of a conventional local oxidation of silicon (LOCOS) process. Next, a gate oxide 54 is formed on substrate 52. The surface of the substrate 52 is then conditioned or pretreated so that the subsequently formed layer 64 of polycrystalline silicon 66 has a smooth morphology. The surface of the substrate 52 is pretreated by implanting hydrogen ions into the surface of the substrate 52 through plasma source ion implantation by the method described above. Fig. 2A shows a layer 64 of polysilicon 66 having been formed on the surface of the substrate 52. The layer 64 of polysilicon 66 covers the gate oxide 54.

As shown in Fig. 2B, after the layer 64 of polycrystalline silicon 66 has been formed on the surface of the substrate 52, the layer 64 is etched to form the gate electrode 70. The gate electrode 70 is formed by any conventional masking and etching techniques currently in use in the art.

As shown in Fig. 2C, the source 56 and the drain 58 are formed by any conventional conductive doping technique currently in use in the art. Desirably, the source 56 and the drain 58 are formed by a self aligned technique. After the source 56 and the drain 58 have been formed, a layer 80 of a dielectric material 68 is formed on the gate 54 and over the source 56 and drain 58. Typically, but not necessarily, the layer 80 will be a layer of an oxidized material and is provided at a thickness such that it serves as an insulating layer. Any material used in the art to

form spacers would be useful for forming the layer 80 of dielectric material 68. Desirably, the dielectric material 68 is silicon dioxide or silicon nitride. The resulting field effect transistor 50 is shown in Fig. 2.

The field effect transistor 50 may also be used in a typical memory array, such as, for example, a static random access memory (SRAM) array or a dynamic random access memory (DRAM) array 100, which is shown in Fig. 3. The DRAM array 100 comprises a plurality of memory cells 102 arranged in rows and columns. As shown in Fig. 3A, each of the memory cells 102 includes at least one field effect transistor 50 and one capacitor 104. The field effect transistor 50 may be the field effect transistor 50, described above and shown in Fig. 2. The method for forming the field effect transistor 50 is described above in connection with the description of Figs. 2A to 2C. Each field effect transistor 50 is coupled to a capacitor 104. The gate of the field effect transistor 50 is coupled to a word line 106 via an interconnect structure. It should be apparent that other devices such as other transistors, bipolar transistors, resistors, other capacitors and the like, may be interconnected with the field effect transistor 50.

The field effect transistor 50 of the present invention may also used in the fabrication of a wafer W, as is shown in Fig. 4. The wafer W includes a plurality of individual die 150 formed on a semiconductor substrate, such as substrate 52. Wafer masks (not shown) are used to apply a desired circuit structure on each of the individual die 150. The desired circuit structure may comprise any of the above described structures, e.g., the DRAM array 100 or an SRAM array. The wafer W is processed using standard wafer fabrication techniques.

The semiconductor device precursor 10 and the method of the present invention are particularly useful in forming thin film transistors and, particularly, thin film transistors which are used to make flat panel displays. By providing the layer of polycrystalline silicon with a smoother morphology, a thinner layer of polycrystalline silicon is formed on the substrate. The final structure of the thin film transistor would be thinner due to the thinner polycrystalline silicon layer and to the layers which are

subsequently deposited on the polycrystalline silicon also being thinner.

A thin film transistor 200 is shown in cross section in Fig. 3. The thin film transistor 200 includes an insulating substrate 202. A layer 204 of a semiconducting material 206 is formed on the surface of the substrate 202. A source region 208 and a drain region 210 are formed on the layer 204 of semiconducting material 206. A layer 212 of a dielectric material 214 is formed on the layer 204 of semiconducting material 206 and covers the source 208 and the drain 210. A layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214 to form a gate electrode 220.

The insulating substrate 202 can be any material used to form insulating layers in semiconductor devices and is preferably glass, quartz or silicon dioxide. Rather than doping a layer of silicon dioxide which is subsequently deposited on a substrate as when forming a field effect transistor and as described above, when the thin film transistor 200 is being formed, the insulating substrate 202, itself, is doped with hydrogen ions by the plasma source ion implantation technique described above.

After the insulating substrate 202 has been doped with hydrogen ions, the layer 204 of semiconducting material 206 is formed on the substrate 202 by any conventional deposition process. Useful deposition methods include, but are not limited to, thermal oxidation, CVD, LPCVD, PECVD, MOCVD and sputtering. Desirably, the layer 204 is deposited by a thermal oxidation process. The layer 204 of semiconducting material 206 can be any material used to form semiconducting layers, including, but are not limited to, gallium arsenide, indium phosphide, polycrystalline silicon, and germanium. Desirably, the layer 204 of semiconducting material 206 is formed from polycrystalline silicon. Once the layer 204 of semiconducting material 206 has been formed, the layer 204 is etched to isolate the various regions of semiconducting material from each other on the surface of the substrate 202.

After the various regions of semiconducting material 204 have been

formed on the substrate 202, the source region 208 and the drain region 210 are formed on the layer 204 of semiconducting material 206. The source region 208 and the drain region 210 can either be formed in the layer 204 of semiconducting material 206 or formed in the layer 212 of dielectric material 214. The source region 208 and the drain region 210 are formed by any doping technique currently in use in the art. The layer 212 of dielectric material 214 is deposited on the layer 204 of semiconducting material 206. Useful deposition methods include, but are not limited to, thermal oxidation, CVD, LPCVD, PECVD, MOCVD and sputtering. The layer 212 of dielectric material 214 can be any material used in the semiconductor manufacturing art to form dielectric layers. Desirably, the dielectric material 214 is silicon dioxide or silicon nitride.

As a final step, a layer 216 of a conducting material 218 is formed on the layer 212 of dielectric material 214. The layer 216 is formed in any manner currently used in the art to form such layers. Useful deposition methods include, but are not limited to, thermal oxidation, CVD, LPCVD, PECVD, MOCVD and sputtering. The conducting material 218 is selected from the group consisting of polycrystalline silicon, metal and any conducting material. The layer 216 of conducting material 218 forms the gate electrode 220.

One skilled in the art will appreciate that the method of the present invention can be carried out as a stand-alone process, clustered as part of the semiconductor manufacturing process or as an in situ pretreatment.

Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention which is defined in the appended claims.

What is claimed is:

CLAIMS

1. A method for controlling the morphology of deposited silicon on a silicon dioxide substrate comprising the steps of:

providing a layer of silicon dioxide;

implanting hydrogen ions into said layer of silicon dioxide by plasma source ion implantation; and

forming a layer of polycrystalline silicon on said layer of silicon dioxide.

2. A method for pretreating silicon dioxide comprising the steps of:

providing a layer of silicon dioxide; and

implanting hydrogen ions into a surface of said layer of silicon dioxide by plasma source ion implantation.

3. A method for forming a semiconductor device precursor comprising the steps of:

providing a semiconductor substrate;

forming a layer of silicon dioxide on said semiconductor substrate;

implanting hydrogen ions by plasma source ion implantation into said layer of silicon dioxide; and

forming a layer of polycrystalline silicon on said layer of silicon dioxide.

4. A method for forming a semiconductor device precursor comprising the steps of:

providing a semiconductor substrate;

forming a layer of silicon dioxide on said semiconductor substrate;

exposing said semiconductor substrate to a hydrogen plasma containing hydrogen ions; and

applying a high voltage pulse to said semiconductor substrate thereby implanting hydrogen ions from said ionized hydrogen plasma into a surface of said

layer of silicon dioxide so that a subsequently formed layer of polycrystalline silicon has a smooth morphology.

5. A method for forming a semiconductor device precursor comprising the steps of:

providing a semiconductor substrate;

forming a layer of silicon dioxide on said semiconductor substrate;

exposing said semiconductor substrate to a hydrogen plasma containing hydrogen ions;

applying a high voltage pulse to said semiconductor substrate to implant hydrogen ions from said ionized hydrogen plasma into a surface of said layer of silicon dioxide so that a subsequently formed layer of polycrystalline silicon has a smooth morphology; and

forming a polycrystalline silicon film on said surface of said layer of silicon dioxide.

6. A method for forming a semiconductor device comprising the steps of:

providing a semiconductor substrate;

forming a layer of silicon dioxide on said semiconductor substrate;

implanting hydrogen ions by plasma source ion implantation into said layer of silicon dioxide; and

forming a layer of polycrystalline silicon on said layer of silicon dioxide.

7. A method for forming a field effect transistor comprising the steps of:

providing a semiconductor substrate having a layer of silicon dioxide formed thereon;

implanting hydrogen ions by plasma source ion implantation into said layer of silicon dioxide;

forming a layer of polycrystalline silicon on said layer of silicon dioxide; and

forming a source, a drain and a gate in said semiconductor substrate.

8. A method for forming a memory array, said memory array comprising a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor, said method comprising the steps of:

providing a semiconductor substrate;

forming a layer of silicon dioxide on at least a portion of said semiconductor substrate;

implanting hydrogen ions into at least a portion of said layer of silicon dioxide by plasma source ion implantation;

forming a layer of polycrystalline silicon over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted; and

forming a gate, a source and a drain for each of said field effect transistors, on said semiconductor substrate.

9. A semiconductor device precursor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on said semiconductor substrate, said layer of silicon dioxide having been doped with hydrogen ions deposited by a plasma source ion implantation process to provide a layer of polycrystalline silicon, which is subsequently deposited on said layer of silicon dioxide with a smooth morphology; and

a layer of polycrystalline silicon formed on said layer of silicon dioxide.

10. A field effect transistor comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted therein by plasma source ion implantation;

a layer of polycrystalline silicon formed on at least a portion of said layer of silicon dioxide; and

a source, a drain and a gate formed in said semiconductor substrate to form a field effect transistor.

11. A memory array comprising:

a semiconductor substrate;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted;

a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor; and

a gate, a source and a drain for each of said field effect transistors formed on said semiconductor substrate.

12. A semiconductor wafer comprising:

a wafer including a semiconductor substrate, said wafer being divided into a plurality of die;

a layer of silicon dioxide formed on at least a portion of said semiconductor substrate, on each of said plurality of die said layer of silicon dioxide having hydrogen ions implanted into at least a portion of said layer of silicon dioxide by plasma source ion implantation;

a layer of polycrystalline silicon formed over at least said portion of said layer of silicon dioxide into which said hydrogen ions were implanted; and

a repeating series of gates, sources and drains for at least one field effect transistor formed on each of said plurality of die, said series of gates, sources and drains being formed on said semiconductor substrate.

13. A method for forming a thin film transistor comprising the steps of:

providing a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass;

forming a layer of a gate oxide material in said semiconductor substrate;

implanting, by plasma source ion implantation, hydrogen ions into a surface of said semiconductor substrate;

forming a layer of polycrystalline silicon on said surface of said semiconductor substrate;

forming a layer of an insulating material on said layer of polycrystalline silicon;

forming a source region and a drain region; and

forming a gate electrode on said layer of insulating material.

14. A thin film transistor comprising:

a semiconductor substrate formed from a material selected from the group consisting of silicon dioxide, quartz and glass, said semiconductor substrate having hydrogen ions implanted therein by plasma source ion implantation;

a layer of polycrystalline silicon formed on at least a portion of semiconductor substrate;

a layer of a insulating material formed on at least a portion of said layer of polycrystalline silicon;

a source region and a drain region formed on said layer of polycrystalline silicon; and

a gate electrode formed on said layer of insulating material.

ABSTRACT OF THE INVENTION

A method for controlling the morphology of deposited silicon on a layer of silicon dioxide and semiconductor devices incorporating such deposited silicon are provided. The method comprises the steps of: providing a layer of silicon dioxide; implanting hydrogen ions into the layer of silicon dioxide by plasma source ion implantation; and forming a layer of polycrystalline silicon on the layer of silicon dioxide.

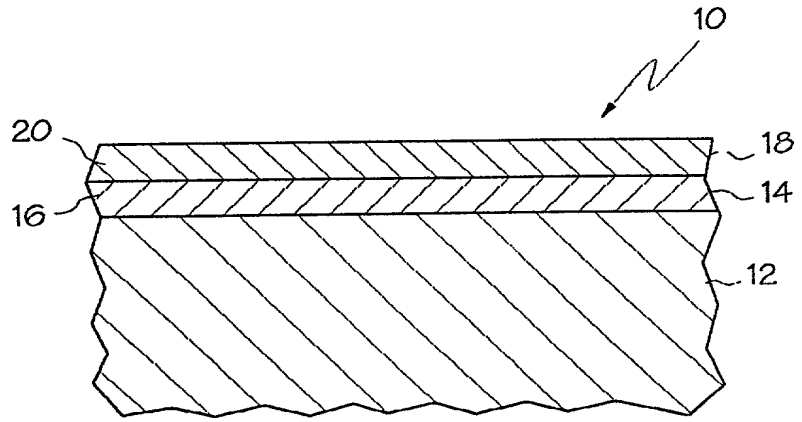

FIG. 1

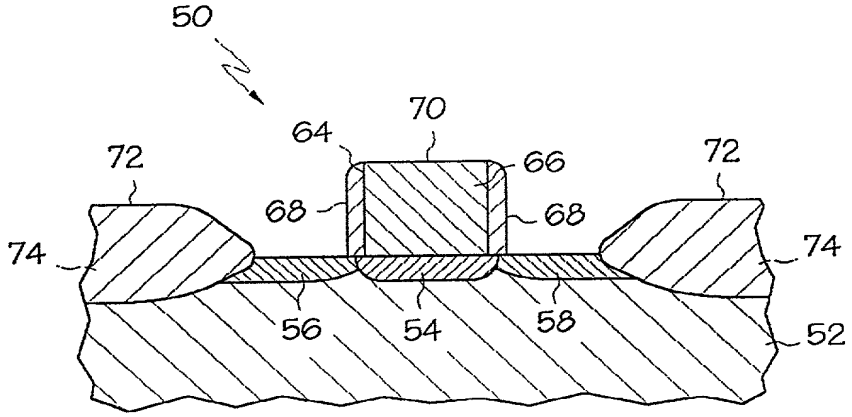

FIG. 2

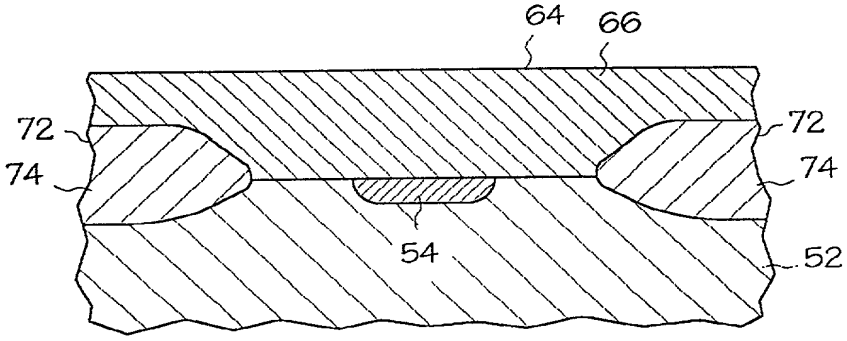

FIG. 2A

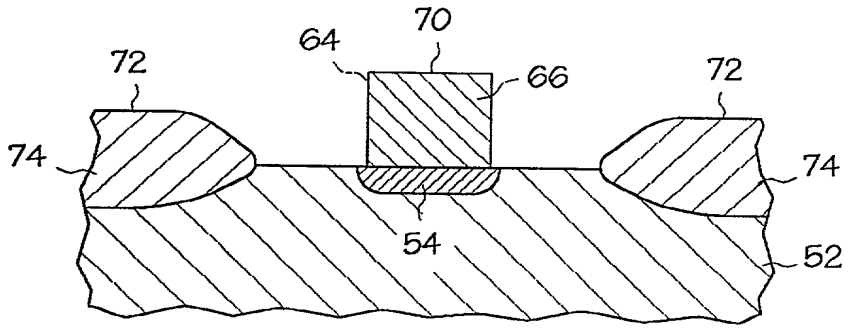

FIG. 2B

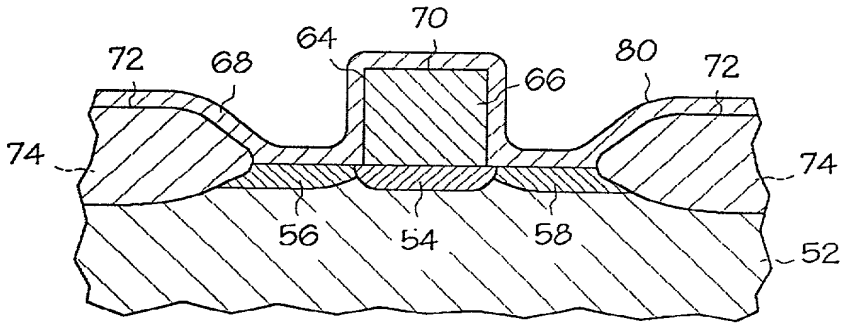

FIG. 2C

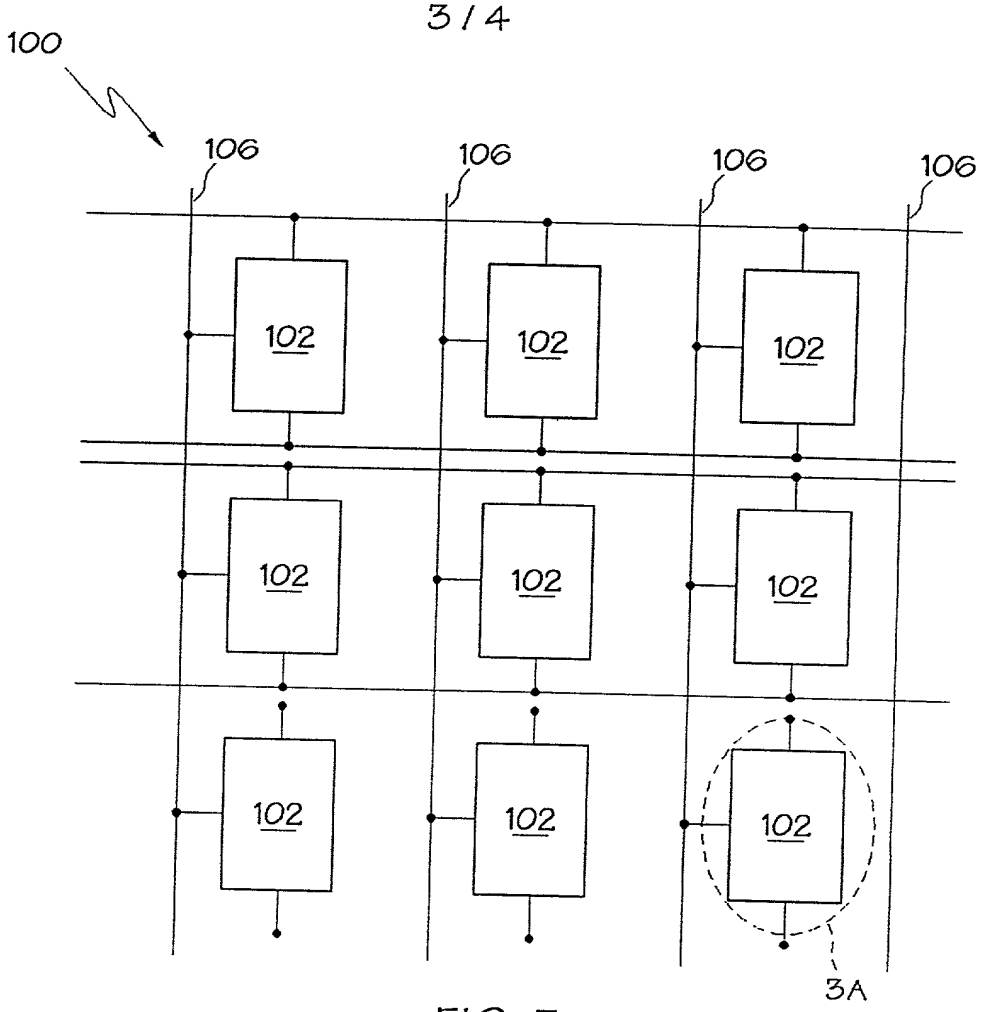
100
106
106
106
106
102
102
102
102
102
102
102
102
102
3A

FIG. 3

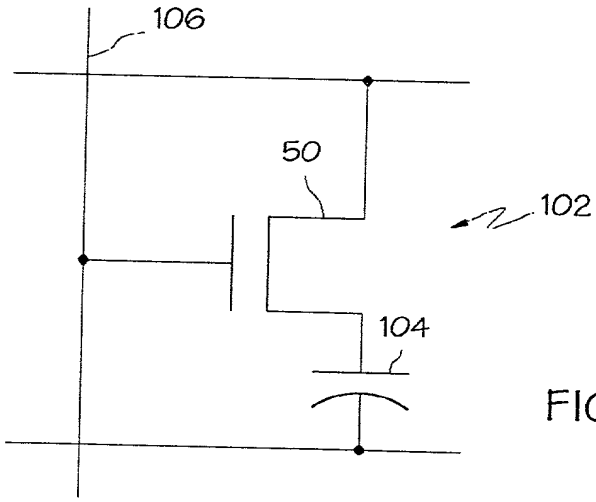
106
50
102
104

FIG. 3A

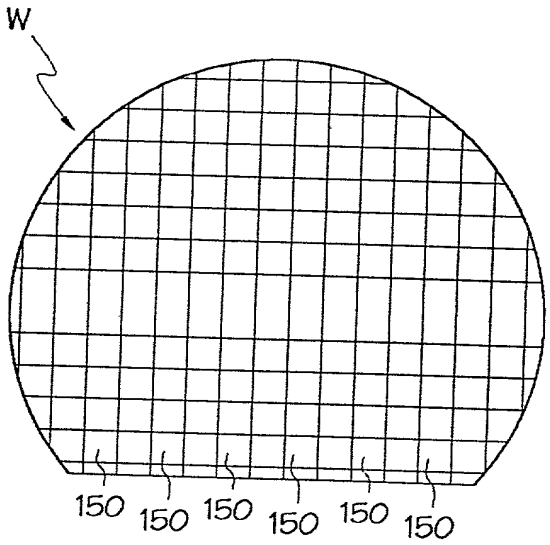
W
150
150
150
150
150
150

FIG. 4

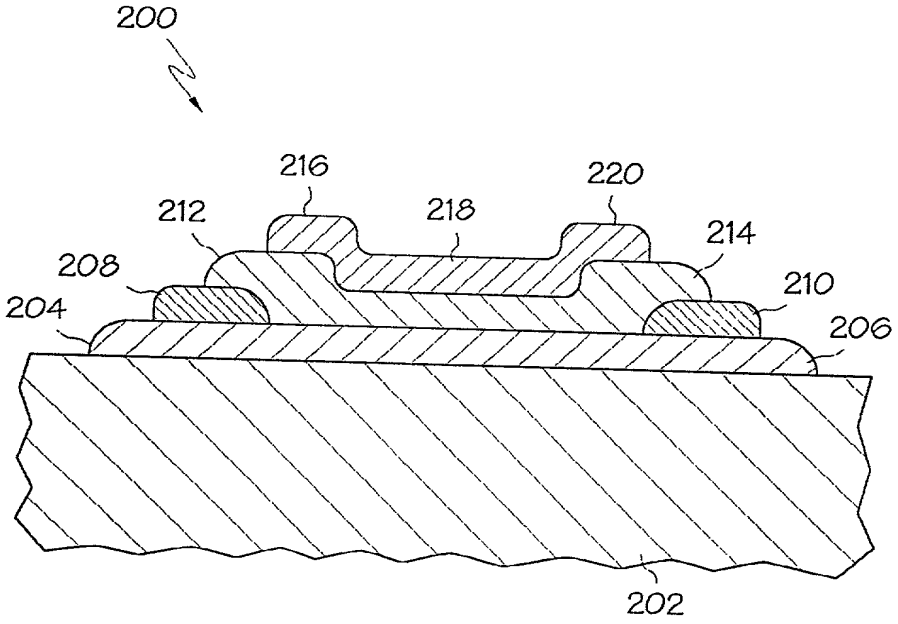
200
216
220
212
218
214
208
210
204
206
202

FIG. 5

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: **METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON**(Docket MIO 037 PA), described and claimed

__X__ in the attached specification;
_____ in the specification filed _____, as U.S. Application Serial No. _____, and as amended _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as filed and as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of sole or first Inventor: David L. Chapek

Inventor's signature David L Chapek

Date: 4/30/98

Residence: ~~33~~ 35 Dec 4/24/98 Sullivan Street
Nashua, NH 03060

Citizenship: USA

Post Office Address: c/o Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83706-9632

The undersigned (whose title is supplied below) is empowered to sign this certificate on behalf of the assignee.

Micron Technology , Inc. hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Richard A. Killworth	Reg. No. 26,397
James F. Gottman	Reg. No. 27,262
Timothy W. Hagan	Reg. No. 29,001
Richard C. Stevens	Reg. No. 28,046
Robert L. Showalter	Reg. No. 33,579
Susan M. Luna	Reg. No. 38,769
James E. Beyer	Reg. No. 39,564
Bradley A. Keller	Reg. No. 37,654
Stephen A. Calogero	Reg. No. 41,491
Charlotte L. Barney	Reg. No. 35,060
Michael L. Lynch	Reg. No. 30,871
Lia M. Pappas	Reg. No. 34,095

Address all telephone calls to (937) 223-2050. Address all correspondence to: KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, L.L.P., One Dayton Centre, One South Main Street, Suite 500, Dayton, Ohio 45402-2023.

Micron Technology, Inc. hereby declares that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: May 1, 1998

Name: Michael L. Lynch

Title: Chief Patent Counsel

Signature: _____

POWER OF ATTORNEY

Applicants: David L. Chapek

Application No.: _____ Filed: _____

Entitled: **METHOD FOR CONTROLLING THE MORPHOLOGY OF DEPOSITED SILICON ON A SILICON DIOXIDE SUBSTRATE AND SEMICONDUCTOR DEVICES INCORPORATING SUCH DEPOSITED SILICON**

CERTIFICATE UNDER 37 CFR 3.73(b)

Micron Technology, Inc., a corporation of the State of Delaware, with a place of business at 8000 S. Federal Way, Boise, ID 83706-9632 certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application identified above, a copy of which is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignee as shown below:

1. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____
   The document was recorded in the Patent and Trademark Office at Reel _____ Frame _____, or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.